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## Microprogram Scheme for Automatic Recovery from Computer Error

A new microprogram scheme enables a computer to recover from a failure in one of its two central processing units during the time duration of the instruction in which the failure occurs. Besides relieving the programmer of the responsibility for a large part of all failure-recovery tasks, the microprogram scheme has the following advantages: 1) built-in interpretive capability, 2) selection of processing interrupts by priority, and 3) economical implementation of a sophisticated bootstrap sequence.

The microprogram scheme is currently incorporated into the digital computation element of a newly developed inertial reference unit. The scheme enables the computer to perform, with a reasonable economy of logic, certain complex calculations. These involve converting certain rotation and acceleration data from a body-referenced coordinate system to an inertial reference system. However, sufficient capacity is reserved to permit the computer to perform instrumentation evaluations, manage a priority-structured real-time command executive system, and communicate with various peripheral devices.

Five operation codes are used in the microprogram to execute control pulses, generate constant data, go to or call microprogram routines, and do one-word memory-to-memory transfers. Available subroutines can be nested (up to eight levels), using a push-down list for return addresses.

### Note:

Requests for further information may be directed to:

Technology Utilization Officer  
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Houston, Texas 77058  
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### Patent status:

No patent action is contemplated by NASA.

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